WHAT IS CLAIMED IS:

1. A transistor, comprising:

a workpiece;

a doped region disposed in the workpiece, the doped region including a dopant species;

a doped gate dielectric disposed over the doped region of the workpiece, the doped gate dielectric including the dopant species;

a gate disposed over the gate dielectric; and

a source region and a drain region formed in at least the doped region of the workpiece, wherein the source region, drain region, gate, and doped gate dielectric comprise a transistor.

2. The transistor according to Claim 1, wherein the dopant species comprises at least one Group V, VI or VII element.

3. The transistor according to Claim 2, wherein the dopant species comprises nitrogen or fluorine.

4. The transistor according to Claim 1, wherein the doped region comprises a thickness of about 100 Å or less.

5. The transistor according to Claim 1, wherein the dopant species fills vacancies in the atomic structure of the gate dielectric.

6. The transistor according to Claim 1, wherein the doped gate dielectric comprises a high k dielectric material or an oxide, and wherein the gate comprises a semiconductor material or a metal.

7. The transistor according to Claim 6, wherein the doped gate dielectric comprises about 50 Å or less of Si_3N_4, Al_2O_3, Ta_2O_5, HfO_2, TiO_2, $HfSiO_x$, ZrO_2, or $ZrSiO_x$.

8. The transistor according to Claim 1, further comprising a thin insulating layer disposed between the gate dielectric and the doped region of the workpiece.

9. The transistor according to Claim 8, wherein the thin insulating layer comprises a thickness of about 10 Å or less.

10. The transistor according to Claim 9, wherein the thin insulating layer comprises silicon dioxide or silicon oxynitride.

11. The transistor according to Claim 1, wherein the workpiece comprises a silicon-on-insulator (SOI) wafer.

12. A method of fabricating a transistor, the method comprising:

providing a workpiece;

introducing a dopant species into the workpiece to form a doped region in the workpiece;

depositing a gate dielectric material over the doped region of the workpiece;

depositing a gate material over the gate dielectric material;

patterning the gate material and gate dielectric material to form a gate and a gate dielectric over the doped region of the workpiece;

transferring the dopant species from the workpiece to the gate dielectric material to form a doped gate dielectric material; and

forming a source region and a drain region in at least the doped region of the workpiece, wherein the source region, drain region, gate, and doped gate dielectric comprise a transistor.

13. The method according to Claim 12, wherein introducing the dopant species comprises introducing at least one dopant species comprising a Group V, VI or VII element into the workpiece.

14. The method according to Claim 13, wherein introducing the dopant species into the workpiece to form the doped region includes introducing nitrogen or fluorine into the workpiece.

15. The method according to Claim 12, wherein introducing the dopant species into the workpiece to form the doped region comprises implanting ions of the dopant species into the workpiece.

16. The method according to Claim 15, wherein implanting the ions of the dopant species comprises an energy level of about 5 KeV or less.

17. The method according to Claim 15, wherein implanting the ions of the dopant species comprises an implantation dose of about 1 x 10^{14} to 1 x 10^{15} ions/cm^2.

18. The method according to Claim 12, wherein transferring the dopant species from the workpiece to the gate dielectric material comprises an anneal process.

19. The method according to Claim 18, wherein the anneal process comprises a temperature of about 900 to 1050 °C.

20. The method according to Claim 18, wherein the anneal process comprises a spike anneal process or a rapid thermal anneal (RTA) process.

21. The method according to Claim 18, wherein the anneal process comprises an anneal process to form the source region and the drain region, or a separate anneal process.

22. The method according to Claim 21, wherein the separate anneal process is performed after depositing the gate dielectric material, after depositing the gate material, or after patterning the gate material and the gate dielectric material.

23. The method according to Claim 12, wherein introducing the dopant species into the workpiece to form the doped region comprises forming a doped region having a thickness of about 100 Å or less.

24. The method according to Claim 12, wherein depositing the gate dielectric material comprises forming vacancies in the atomic structure of the gate dielectric material, and wherein transferring the dopant species from the workpiece to the gate dielectric material comprises filling the vacancies of the gate dielectric material.

25. The method according to Claim 12, wherein depositing the gate dielectric material comprises depositing a high k dielectric material or an oxide, and wherein depositing the gate material comprises depositing a semiconductor material or a metal.

26. The method according to Claim 12, wherein depositing the gate dielectric comprises depositing about 50 Å or less of Si_3N_4, Al_2O_3, Ta_2O_5, HfO_2, TiO_2, $HfSiO_x$, ZrO_2, or $ZrSiO_x$.

27. The method according to Claim 12, wherein depositing the gate dielectric comprises atomic layer deposition (ALD), chemical vapor deposition (CVD), or metal oxide CVD (MOCVD).

28. The method according to Claim 12, further comprising forming a thin insulating layer over the doped region of the workpiece, before introducing the dopant species into the workpiece to form the doped region.

29. The method according to Claim 28, wherein forming the thin insulating layer comprises depositing an insulating layer having a thickness of about 100 Å or less.

30. The method according to Claim 28, wherein forming the thin insulating layer comprises forming silicon dioxide or silicon oxynitride.

31. The method according to Claim 28, further comprising removing at least a portion of the thin insulating layer, after introducing the dopant species into the workpiece to form the doped region.

32. The method according to Claim 31, wherein about 10 Å or less of the thin insulating layer remains over the doped region of the workpiece, after removing at least the portion of the thin insulating layer.

33. The method according to Claim 31, wherein removing at least a portion of the thin insulating layer comprises removing all of the thin insulating layer.

34. The method according to Claim 12, wherein providing the workpiece comprises providing a silicon-on-insulator (SOI) wafer.

35. The method according to Claim 12, further comprising, before depositing the gate dielectric material:

depositing a dummy gate material over the workpiece;

patterning the dummy gate material with the pattern of the gate;

forming the source region and the drain region; and

removing the dummy gate material.

36. The method according to Claim 35, wherein introducing the dopant species into the workpiece to form a doped region is performed either before or after forming the source region and the drain region.